New patent claims 1 to 19

1. A semiconductor component
- having a semiconductor substrate and an insulating layer formed on the semiconductor substrate, and
- having a capacitance structure which is formed in the insulating layer, the capacitance structure having at least two metallization planes (1 to 7) for producing a first part of a capacitance surface which extend essentially parallel to the substrate surface and are each electrically connected to one of two connecting lines, where
- the capacitance structure has at least one electrically conductive region (1a to 1j; 2a to 2j; 31a to 36a; 41a to 46a; 5a to 5f) which is designed to produce a second part of the capacitance surface between the metallization planes (1 to 7) in the insulating layer, and
- the electrically conductive region (1a to 1j; 2a to 2j; 31a to 36a; 41a to 46a; 5a to 5f) is electrically connected only to one of the metallization planes (1 to 7),

characterized in that
- the electrically conductive region (1a to 1j; 2a to 2j; 31a to 36a; 41a to 46a; 5a to 5f) is in the form of a homogeneous, cohesive elevation.

2. The semiconductor component as claimed in claim 1, characterized in that
- the electrically conductive regions (1a to 1j; 2a to 2j; 31a to 36a; 41a to 46a; 5a to 5f) are areas produced using a Damascene process.

3. The semiconductor component as claimed in claim 1 or 2,
characterized in that

the electrically conductive region (1a to 1j; 2a to 2j; 31a to 36a; 41a to 46a; 5a to 5f) is arranged essentially at right angles to the metallization planes (1 to 7).

4. The semiconductor component as claimed in one of the preceding claims,
characterized in that
each of the two metallization planes (1, 2) is in the form of a cohesive plate and is connected to at least one respective electrically conductive region (1a to 1j; 2a to 2j).

5. The semiconductor component as claimed in claim 4, characterized in that
the first metallization plane (1) is connected to a plurality of first electrically conductive regions (1a to 1j) which are in bar form, and the second metallization plane (2) is connected to a plurality of second electrically conductive regions (2a to 2j) which are in bar form.

6. The semiconductor component as claimed in claim 5, characterized in that
the first bar-like, electrically conductive regions (1a to 1j) are arranged at a fixed distance (a) from one another on the first metallization plane (1) and extend in the direction of the second metallization plane (2), and the second bar-like, electrically conductive regions (2a to 2j) are arranged at a fixed distance (a) from one another on the second metallization plane (2) such that they respectively extend between the first bar-like regions (1a to 1j) in the direction of the first metallization plane (1).

7. The semiconductor component as claimed in claim 6, characterized in that
the first bar-like regions (1a to 1j) have a first length L_1, the second bar-like regions (2a to 2j)

have a second length L_2, with the length L_2 being greater than, less than or the same as the length L_1, and the sum of the lengths L_1 and L_2 of a first and of a second bar-like region (1a to 1j; 2a to 2j) is greater than a distance (b) between the two metallization planes (1, 2).

8. The semiconductor component as claimed in one of claims 1 to 3,
characterized in that
the two metallization planes (3, 4) are respectively constructed from at least two electrical lines (31 to 36; 41 to 46) arranged parallel to one another, and the electrical lines (31 to 36) in the first metallization plane (3) are arranged congruently with respect to the electrical lines (41 to 46) in the second metallization plane (4).

9. The semiconductor component as claimed in claim 8, characterized in that
each of the first and second electrical lines (31 to 36; 41 to 46) respectively has at least one electrically conductive region (31a to 36a; 41a to 46a) arranged on it.

10. The semiconductor component as claimed in claim 9, characterized in that
a plurality of first electrically conductive regions (31a to 36a) which are in bar form are arranged at the fixed distance (c) from one another on each of the first electrical lines (31 to 36) and extend in the direction of the second electrical lines (41 to 46), and a plurality of second electrically conductive regions (41a to 46a) which are in bar form are likewise arranged at the fixed distance (c) but offset from the first electrically conductive regions (31a to

36a) on each of the second electrical lines (41 to 46) and extend between the first bar-like electrically conductive regions (31a to 36a) in the direction of the first electrical lines (31 to 36).

11. The semiconductor component as claimed in claim 10,
characterized in that
the bar-like first regions (31a to 36a) have a first length L_1, the bar-like second regions (41a to 46a) have a second length L_2, with the length L_2 being greater than, less than or the same as the length L_1, and the sum of the lengths L_1 and L_2 of a first and of a second bar-like region (31a to 36a; 41a to 46a) is greater than the distance (d) between the electrical lines (31 to 36; 41 to 46).

12. The semiconductor component as claimed in one of claims 1 to 3,
characterized in that
one of the two metallization planes (5) is in the form of a cohesive plate, and the second metallization plane (6) is in the form of a lattice.

13. The semiconductor component as claimed in claim 12,
characterized in that
the metallization plane (5) which is in the form of a cohesive plate has at least one electrically conductive region (5a to 5f) which is in bar form arranged on it which extends in the direction of the second lattice-like metallization plane (6) and projects at least partially into a cutout in the lattice-like metallization plane (6).

14. The semiconductor component as claimed in either of claims 12 and 13,

characterized in that
a lattice-like third metallization plane (7) is arranged parallel to and at a distance from the second metallization plane (6)
on said metallization plane (6), and the second and third metallization planes (6, 7) are electrically connected to one another by means of electrical connections (61).

15. The semiconductor component as claimed in claim 14,
characterized in that

the bar-like, electrically conductive regions (5a to 5f) are in a form such that they project through the cutouts in the second metallization plane (6) and extend at least partially into the cutouts in the third metallization plane (7).

16. A method for fabricating a semiconductor component, in which an insulating layer is deposited on a semiconductor substrate, and a capacitance structure (K) is produced in the insulating layer, the capacitance structure (K) having at least two metallization planes (1 to 7) which are formed essentially parallel to the substrate surface,
characterized in that
an electrically conductive, homogeneous region (1a to 1j; 2a to 2j; 31a to 36a; 41a to 46a; 5a to 5f) is formed in the insulating layer between the metallization planes (1 to 7), and the electrically conductive region (1a to 1j; 2a to 2j; 31a to 36a; 41a to 46a; 5a to 5f) is electrically connected only to one of the metallization planes (1 to 7).

17. The method as claimed in claim 16,
characterized in that
the electrically conductive region (1a to 1j; 2a to 2j; 31a to 36a; 41a to 46a; 5a to 5f) is in the form of a homogeneous cohesive elevation, the electrical region (1a to 1j; 2a to 2j; 31a to 36a; 41a to 46a; 5a to 5f) being formed without such a metal area, which can be produced by patterning a metallization plane (1 to 7).

18. The method as claimed in either of claims 16 and 17,
characterized in that

the electrically conductive region (1a to 1j; 2a to 2j; 31a to 36a; 41a to 46a; 5a to 5f) in the insulating layer is in the form of a via structure.

19. The method as claimed in one of claims 16 to 18, characterized in that
the electrically conductive region (1a to 1j; 2a to 2j; 31a to 36a; 41a to 46a; 5a to 5f) is formed essentially at right angles to the metallization planes (1 to 7).